WHAT IS CLAIMED IS:

1. A test access port comprising:

a fastdata register that is selectably connectable to a data register to form at least a portion of a TDI-to-TDO path, said fastdata register configured to operate such that a fastdata access completes when a processor access is pending and said processor access is to a predetermined area of dmseg memory.

2. The test access port of claim 1, further comprising a data register serially coupled to said fastdata register.

3. The test access port of claim 1, wherein said fastdata register is configured to operate such that an attempt to complete said fastdata access occurs by clearing said fastdata register.

4. The test access port of claim 1, wherein said fastdata register is configured to operate such that said fastdata register is set to indicate that said fastdata access will complete.

5. The test access port of claim 1, wherein said fastdata register is configured to operate such that, if said processor access is not pending, said fastdata register is cleared to indicate that said fastdata access will not complete.

6. The test access port of claim 5, wherein said fastdata register is configured to operate such that, if a PrAcc bit is asserted while said processor access is not pending, said fastdata register is cleared to indicate that said fastdata access will not complete.

7. The test access port of claim 1, wherein said fastdata register is configured to operate such that, if said processor access is outside said predetermined area of dmseg memory, said fastdata register is cleared to indicate that said fastdata access will not complete.

8. A method for transferring a plurality of data words between a test probe and a target processor over a serial link, the method comprising:

directing the target processor to configure a test data in port to test data out port ("TDI-to-TDO") path to include a data register and a fastdata register;

without reconfiguring said TDI-to-TDO path, shifting each of the plurality of data words accompanied by a SPrAcc bit into said data register and said fastdata register of said TDI-to-TDO path, respectively, said SPrAcc bit indicative of a request for completion of a pending processor access.

9. The method of claim 8, further comprising receiving an indication from said TDI-to-TDO path whether said pending processor access completed.

10. The method of claim 9, wherein said receiving an indication comprises receiving an indication that said pending processor access successfully completed when a processor access

was pending at a time of said request and said processor access was to a predetermined area of a dmseg memory.

11. The method of claim 9, wherein said receiving an indication comprises receiving an indication that said pending processor access failed to complete when a processor access was not pending at a time of said request.

12. The method of claim 9, wherein said receiving an indication comprises receiving an indication that said pending processor access failed to complete when a processor access was outside a predetermined area of dmseg memory.

13. A method for transferring a plurality of data words between a test probe and a target processor over a serial link, the method comprising:

configuring a test data in port to test data out port ("TDI-to-TDO") path to include a data register and a fastdata register;

receiving from the test probe one of the plurality of data words accompanied by an SPrAcc bit in said data register and said fastdata register of said TDI-to-TDO path, respectively, said SPrAcc bit indicating a request for completion of a pending processor access; and

indicating to the test probe whether said pending processor access completed.

14. The method of claim 13, wherein said indicating comprises indicating to the test probe that said pending processor access successfully completed when a processor access was pending at a time of said request and said processor access was to a fastdata area of a dmseg memory.

15. The method of claim 13, wherein said indicating comprises indicating to the test probe that said pending processor access failed to complete when a processor access was not pending at a time of said request.

16. The method of claim 13, wherein said indicating comprises indicating to the test probe that said pending processor access failed to complete when a processor access was outside a fastdata area of a dmseg memory.

17. The method of claim 13, further comprising stalling on an attempt to access a fastdata area of dmseg memory.

18. A method for transferring a plurality of data words between a test probe and a target processor over a link, the method comprising:

requesting a serial data transfer;

receiving control information in said serial data transfer, said control information indicative of a request for completion of a processor access; and

confirming said processor access is pending and a target address associated with said processor access falls within a predetermined acceptable range of memory addresses.

19. The method of claim 18 further comprising enabling said serial data transfer upon successfully confirming said processor access is pending and said target address associated with

said processor access falls within a predetermined acceptable range of memory addresses for one of said plurality of data words.

20. The method of claim 19 wherein said confirming said processor access is pending comprises detecting a value of a control bit.

21. The method of claim 20 further comprising resetting said value of said control bit after successfully confirming said processor access is pending.

22. The method of claim 19 wherein said confirming said processor access is pending and a target address associated with said processor access falls within a predetermined acceptable range of memory addresses is achieved without use of the probe.

23. The method of claim 22 wherein said control information is modified to indicate success or failure of confirming said processor access is pending and a target address associated with said processor access falls within a predetermined acceptable range of memory addresses for said one of said plurality of data words.

24. The method of claim 21 wherein said resetting said value of said control bit is achieved without use of the probe.

25. The method of claim 18 further comprising:

in response to direction from the probe, configuring a test-data-in-port to test-data-out-port ("TDI-to-TDO") path to include a data register and a Fastdata register; and

without reconfiguring said TDI-to-TDO path, shifting each of said plurality of data words accompanied by said control information in modified or unmodified form over said TDI-to-TDO path and the link.

26. The method of claim 25 wherein said control information is an SPrAcc bit associated with each of said plurality of data words.

27. The method of claim 26 wherein said configuring TDI-to-TDO path to include a data register and a Fastdata register is achieved in response to receiving a FASTDATA instruction from the probe.

28. A computer-readable medium comprising a programmable device described in software, the programmable device including a test access port comprising:

a Fastdata register that is selectably connectable to a data register to form at least a portion of a test-data-in-port to test-data-out-port path, said Fastdata register configured to operate such that a fastdata access completes when a processor access is pending and said processor access is to a predetermined area of memory.

29. The computer readable medium of claim 28 wherein the programmable device is a microprocessor core.

30. A method for transferring a plurality of data words between a test probe and a target processor over a link, the method comprising:

in response to a request from the target processor for a serial data transfer, including control information in said serial data transfer, said control information indicative of a request for completion of a processor access; and

receiving second control information that confirms said processor access was pending and a target address associated with said processor access falls within a predetermined acceptable range of memory addresses.

31. The method of claim 30 further comprising:

directing that target processor to configure a test-data-in-port to test-data-out-port ("TDI-to-TDO") path to include a data register and a Fastdata register; and

shifting each of said plurality of data words accompanied by said control information in modified or unmodified form over said TDI-to-TDO path and the link.

32. The method of claim 31 wherein said control information is an SPrAcc bit associated with each of said plurality of data words shifted into said TDI-to-TDO path.

33. The method of claim 31 wherein said second control information is an SPrAcc bit associated with each of said plurality of data words shifted out of said TDI-to-TDO path.

34. The method of claim 31 wherein said directing the target processor to configure a TDI-to-TDO path to include a data register and a Fastdata register is achieved by sending a FASTDATA instruction.